IN THE SPECIFICATION:

Please amend the paragraphs in the specification as follows:

[0011] Also preferably, the first signal processing circuit comprises: first integrating circuits, provided in correspondence to the first groups of the photosensitive portions and each converting and outputting the electric currents from the corresponding first groups of the photosensitive portions into and as a voltage; first CDS circuits, disposed in correspondence to the first integrating circuits and each in turn comprising a first coupling capacitance element and a first amplifier, disposed in that order between an output terminal and an input terminal that inputs the voltage from the corresponding first integrating circuit, a first integrating capacitance element, disposed in parallel between the input and the output of the first amplifier, and a first switching element, making charges of an amount corresponding to the variation amount of the voltage be accumulated in the first integrating capacitance element; second CDS circuits, disposed in correspondence to the first integrating circuits and each in turn comprising a second coupling capacitance element and a second amplifier, disposed in that order between an output terminal and an input terminal that inputs the voltage from the corresponding first integrating circuit, a second integrating capacitance element, having a capacitance value equal to the capacitance value of the first integrating capacitance element and disposed in parallel between the input and the output of the second amplifier, and a second switching element, making charges of an amount corresponding to the variation amount of the voltage be accumulated in the second integrating capacitance element; and first difference operational circuits, disposed in correspondence to the first CDS circuits and the second CDS circuits and each determining a difference in the amounts of charges respectively accumulated in the first integrating capacitance element of the corresponding first CDS circuit and the second integrating capacitance element of the corresponding second CDS circuit and outputting a voltage that is in accordance with the

difference; and the second signal processing circuit comprises: second integrating circuits, provided in correspondence to the second groups of the photosensitive portions and each converting and outputting the electric currents from the second corresponding group of the photosensitive portions as a voltage; third CDS circuits, disposed in correspondence to the second integrating circuits and each in turn comprising a third coupling capacitance element and a third amplifier, disposed in that order between an output terminal and an input terminal that inputs the voltage from the corresponding second integrating circuit, a third integrating capacitance element, disposed in parallel between the input and the output of the third amplifier, and a third switching element, making charges of an amount corresponding to the variation amount of the voltage be accumulated in the third integrating capacitance element; fourth CDS circuits, disposed in correspondence to the second integrating circuit and each in turn comprising a fourth coupling capacitance element and a fourth amplifier, disposed in that order between an output terminal and an input terminal that inputs the voltage from the corresponding second integrating circuit, a fourth integrating capacitance element, having a capacitance value equal to the capacitance value of the ~~fourth~~ third integrating capacitance element and disposed in parallel between the input and the output of the fourth amplifier, and a fourth switching element, making charges of an amount corresponding to the variation amount of the voltage be accumulated in the fourth integrating capacitance element; and second difference operational circuits, disposed in correspondence to the third CDS circuits and the fourth CDS circuits and each determining a difference in the amounts of charges respectively accumulated in the third integrating capacitance element of the corresponding third CDS circuit and the fourth integrating capacitance element of the corresponding fourth CDS circuit and outputting a voltage that is in accordance with the difference. With such a composition, since a first difference operational circuit is provided in accordance with each first group of the photosensitive portions and a

second difference operational circuit is disposed in accordance with each second group of the photosensitive portions, the luminance profiles in the first and second directions can be obtained at high speed. Also, even if the first integrating circuits and the second integrating circuits respectively have noise fluctuations that differ according to integrating operation, the noise errors are eliminated by the first to fourth CDS circuits. Also, since charges that are in accordance with the signal light components from the light source and the background light components are accumulated in the first and third integrating capacitance elements of the first and third CDS circuits during the first period, charges that are in accordance with the background light components are accumulated in the second and fourth integrating capacitance elements of the second and fourth CDS circuits during the second period, and differences between the two are determined by the first and second difference operational circuits, the voltages from the first and second difference operational circuits will correspond to just the signal light components from the light source. The S/N ratio of luminance profile detection will thus be excellent even if the intensities of the light made incident on the photosensitive region, in other words, the above-mentioned voltages are low in value.

[0079] In photosensitive region 10, pixels 11_{mn} are arrayed two-dimensionally in ~~M rows and N columns~~ <u>M columns and N rows</u>. One pixel is arranged by adjacently positioning, on the same plane, a photosensitive portion 12_{mn} (first photosensitive portion) and a photosensitive portion 13_{mn} (second photosensitive portion), each outputting a current that is in accordance with the intensity of light incident thereon. Thus in photosensitive region 10, photosensitive portions 12_{mn} and photosensitive portions 13_{mn} are arrayed in a two-dimensionally mixed manner on the same plane.

[0098] As shown in FIG. 11, first integrating circuit 23 comprises an amp A_1, inputting the electric currents from the first groups of the photosensitive portions 12_{mn}, which are

electrically connected across the pluralities of pixels 11_{11} to 11_{1N}, 11_{21} to 11_{2N}, …, 11_{M1} to 11_{MN} aligned in the first direction, and amplifying the charges of the input electric currents, a capacitor C_1, having one terminal connected to the input terminal of amp A_1 and having the other terminal connected to the output terminal of amp A_1, and a switch SW_1, having one terminal connected to the input terminal of amp A_1, having the other terminal connected to the output terminal of amp A_1, being put in the "ON" state when a reset signal Φ_{Hreset} (not shown), output from timing control circuit 50 is ~~significant~~ High, and being put in the "OFF" state when reset signal Φ_{Hreset}, is ~~non-significant~~ Low.

[0108] During the above-mentioned second period, light source 3 is not lit. That is, this is the period during which switch 7 is opened based on the control signal from timing control circuit 50 and spot light is not illuminated from light emitting element 5. Thus of the digital values output from first A/D conversion circuit 25, the digital values corresponding to the ~~first~~ second period are outputs that express the luminance profile in the second direction that contains just the background light components (for example, light from a fluorescent lamp, sun, etc.).

[0114] Second integrating circuit 33 has an composition equivalent to first integrating circuit 23 shown in FIG. 11 and comprises an amplifier, inputting the electric currents from the second groups of the photosensitive portions 13_{mn}, which are electrically connected across the pluralities of pixels 11_{11} to 11_{M1}, 11_{12} to 11_{M2}, …, 11_{1N} to 11_{MN} aligned in the second direction, and amplifying the charges of the input electric currents, a capacitor, having one terminal connected to the input terminal of the amplifier and having the other terminal connected to the output terminal of the amplifier, and a switch, having one terminal connected to the input terminal of the amp, having the other terminal connected to the output terminal of the amplifier, being put in the "ON" state when a reset signal Φ_{Vreset} (not shown), output from timing control

circuit 50 is ~~significant~~ High, and being put in the "OFF" state when reset signal Φ_{Vreset}, is ~~non-significant~~ Low.

[0118] Reset signal Φ_{Vreset} from timing control circuit 50 is input into second integrating circuit 33 (see FIG. 14D ~~FIG. 14E~~). During the period in which reset signal Φ_{Vreset} is in the "OFF" state, the charges accumulated in the corresponding second group of the photosensitive portions 13_{mn} are accumulated in the capacitor and a voltage, which is in accordance with the amount of the accumulated charges, is successively output from second integrating circuit 33 (see FIG. 14I). When reset signal Φ_{Vreset} is in the "ON" state, second integrating circuit 33 closes the switch and initializes the capacitor.

[0141] Second CDS circuits 122 are provided in correspondence to first integrating circuit 23 and each outputs a voltage that is in correspondence to the variation amount of the voltage from the corresponding first integrating circuit 23. As shown in FIG. 19, each second CDS circuit 122 has a switch SW_{221}, a second coupling capacitor C_{221}, and a second amp A_{22}, disposed in that order between an input terminal and an output terminal. Also, a switch SW_{222} and a second integrating capacitor C_{222} are connected in parallel to each other between the input and output of amp A_{22}. Switches SW_{221} and SW_{222} function as second switching element for accumulating charges in second integrating capacitor C_{222}. The capacitance value of second integrating capacitor C_{222} of second CDS circuit 122 is equal to the capacitance value of ~~second~~ first integrating capacitor C_{212} of first CDS circuit 121. When switch SW_{222} is closed, second CDS circuit 122 discharges and initializes second integrating capacitor C_{222}. When switch SW_{222} is opened and switch SW_{221} is closed, second charges, which are input from the input terminal and via second coupling capacitor C_{221}, are accumulated in second integrating capacitor C_{222}, and a voltage that is in accordance with the accumulated charges is output from the output terminal. Switch SW_{221} opens and closes based on a CSW221 signal output from timing control circuit 50.

Also, switch SW_{222} opens and closes based on a Clamp 2 signal output from timing control circuit 50.

[0142] First difference operational circuits 130 are provided in correspondence to first CDS circuits 121 and second CDS circuits 122 and each determines the difference between the respective amounts of charges accumulated in first integrating capacitor C_{212} of the corresponding first CDS circuit 121 and second integrating capacitor C_{222} of the corresponding second CDS circuit [[121]] <u>122</u> and outputs a voltage corresponding to this difference. As shown in FIG. 19, each first difference operational circuit 130 has two input terminals 130a and 130b and a single output terminal 130c, first input terminal 130a is connected to the output terminal of first CDS circuit 121, and second input terminal 130b is connected to the output terminal of second CDS circuit 122. Each first difference operational circuit 130 is equipped with switches SW_{31} to SW_{33}, a capacitor C_3, and an amp A_3. Switch SW_{31}, capacitor C_3, and amp A_3 are disposed in that order between first input terminal 130a and output terminal 130c and switch SW_{32}, capacitor C_3, and amp A_3 are disposed in that order between second input terminal 130b and output terminal 130c. Also, the connection point of capacitor C_3 and amp A_3 is grounded via switch SW_{33}.

[0150] Second difference operational circuits 230 are provided in correspondence to third CDS circuits 221 and fourth CDS circuits 222 and each determines the difference between the respective amounts of charges accumulated in the third integrating capacitor of the corresponding third CDS circuit 221 and the fourth integrating capacitor of the corresponding fourth CDS circuit [[221]] <u>222</u> and outputs a voltage corresponding to this difference. Each second difference operational circuit 230 has a composition equivalent to that of first difference operational circuit 130, shown in FIG. 19, and is equipped with switches, a capacitor, and an amp.

[0151] Second S/H circuits 240 are provided in correspondence to second difference operational circuits 230 and each holds and then outputs the voltage from the corresponding second difference operational circuit 230. Each second S/H circuit 240 has a composition equivalent to that of first S/H circuit 140 shown in FIG. 20, has a switch and an amp disposed in that order between an input terminal and an output terminal, and the connection point of the switch and the amp is grounded via a capacitor. Second switches 260 are closed ~~opened~~ successively by being controlled by second shift register 250 and successively inputs the voltages from second S/H circuits 240 into second A/D conversion circuit 270.

[0169] Also with the photodetector of the second embodiment, first signal processing circuit 20 includes first integrating circuits 23, first CDS circuits 121, second CDS circuits 122, and first difference operational circuits 130, and second signal processing circuit 30 includes second integrating circuits 33, third CDS circuits 221, fourth CDS circuits 222, and second difference operational circuits 230 [[130]]. Since a first difference operational circuit 130 is thus provided for each first group of the photosensitive portions 12_{mn} and a second difference operational circuit 230 is provided for each second group of the photosensitive portions 13_{mn}, the luminance profiles in the first and second directions can be obtained at high speed. Also, even if the respective first integrating circuits 23 and second integrating circuit 33 have noise fluctuations that differ according to integrating operation, the noise errors are resolved by first to fourth CDS circuits 121, 122, 221, and 222, respectively. Also, since charges, corresponding to the spot light components (signal light components) from light source 3 and the background light components, are accumulated in first and third integrating capacitors C_{212} of first and third CDS circuits 121 and 221 in the first period, charges, corresponding to the background light components, are accumulated in second and fourth integrating capacitors C_{222} of second and fourth CDS circuits 122 and 222 in the second period, and the differences between these charges

are determined by first and second difference operational circuits 130 and 230, the voltages from first and second difference operational circuits 130 and 230 correspond to just the spot light components from light source 3. Thus even when the intensity of the light made incident on photosensitive region 10 is low, that is, even if the above-mentioned voltages are small, the S/N ratio of luminance profile detection will be excellent.

[0180] Second charge accumulation circuits 410 are provided in correspondence to the second groups of the photosensitive portions 13_{mn} and each has a third capacitor and a fourth capacitor, disposed in parallel between an output terminal and an input terminal that inputs electric currents from the corresponding second group of the photosensitive portions 13_{mn}, and accumulates charges, which are in accordance with electric currents corresponding to the charges accumulated in the corresponding second group of the photosensitive portions 13_{mn} over the above-mentioned first period, in the third capacitor, and accumulates charges, which are in accordance with electric currents corresponding to the charges accumulated in the corresponding group of photosensitive portions 13_{mn} over the above-mentioned second period, in the fourth capacitor. Each second charge accumulation circuit 410 has a composition equivalent to that of first charge accumulation circuit 310 shown in FIG. 24 and comprises the above-mentioned third capacitor, fourth capacitor, and five switches. ~~As with switches SW_{41A}, SW_{41B}, and SW_{43}, the three switches, disposed between the input terminal and the third and fourth capacitors, open and close based on control signals A, B, and R output from timing control circuit 50.~~ As with switches SW_{41A} and SW_{41B}, the two switches, disposed between the input terminal and the third and fourth capacitors, open and close based on control signals A and B output from timing control circuit 50. As with switch SW_{43}, the switch, disposed between the input terminal and the first reference potential V_{ref1}, open and close based on control signal R output from timing control circuit 50. As with switch SW_{42A} and SW_{42B}, the two switches, disposed between the

output terminal and the third and fourth capacitors, are controlled and successively closed by signals shift(V_{nA}) and shift(V_{nB}), which are output from second shift register 420. As with first shift register 320, second shift register 420 is controlled in its operation by a signal output from timing control circuit 50 and successively closes the respective switches mentioned above.

[0196] Second charge accumulation circuits 410, second shift register 420, second integrating circuit 430, second difference operational circuit 440, and second A/D conversion circuit 270, included in second signal processing circuit 30 perform operations equivalent to those (see FIG. 27) of first charge accumulation circuits 310, first shift register 320, first integrating circuit 330, first difference operational circuit 340, and first A/D conversion circuit 170 of first signal processing circuit 20 and a voltage, of voltage values corresponding to just the spot light components, is output from second difference operational circuit 440 ~~first difference operational circuit 340~~. As mentioned above, the voltage from first difference operational circuit 340 is successively input into second A/D conversion circuit 270 and converted into digital values that are output from second A/D conversion circuit 270.